WHAT IS CLAIMED IS:

1. A semiconductor integrated circuit device comprising:

a plurality of memory cells, each having a storage MOSFET holding an information in a gate of the storage MOSFET, a write transistor supplying a write information voltage corresponding to the information to the gate of the storage MOSFET, and a capacitor having a first terminal and a second terminal;

a plurality of word lines coupled with the plurality of the memory cells; and

a plurality of data lines coupled with the plurality of the memory cells,

wherein the first terminal of the capacitor is coupled with one of the plurality of word lines and the second terminal of the capacitor is coupled with the gate of the storage MOSFET,

wherein, in a read operation of the semiconductor integrated circuit device, the gate voltage of the storage MOSFET is boosted by a transition of the word line from a first voltage to a second voltage greater than the first voltage.

2. A semiconductor integrated circuit device according to claim 1, wherein the plurality of data lines have a plurality of write data lines and a plurality of read data lines,

wherein each of the plurality of the write data lines is coupled with the write transistor included in each of the plurality of memory cells, and

wherein each of the plurality of the read data lines is coupled with the storage MOSFET in each of the plurality of memory cells.

3. A semiconductor integrated circuit device according to claim 2, further comprising:

a plurality of write control circuits connected between the plurality of read data lines and the plurality of write data lines, respectively,

wherein each of the plurality of write control circuits conveys a signal which appeared on a corresponding one of the plurality of read data lines to a corresponding one of the plurality of write data lines.

4. A semiconductor integrated circuit device according to claim 1, further comprising:

a data line select circuit selecting one of the plurality of data lines; and

a first and a second common data line coupled with one of the plurality of the data lines selected by the data line select circuit, wherein the first and second common data lines are precharged to a precharge voltage that is between a high level voltage and a low level voltage at a time of amplifying voltages on the first and the second common data lines, and

wherein a read information which appears on one of the first and second common data lines is amplified using the precharge voltage of the other of the first and second common data lines as a reference voltage.

5. A semiconductor integrated circuit device according to claim 4,

wherein the same number of data lines are respectively coupled with each of the first and second common data lines via the data line select circuit, and

wherein the semiconductor integrated circuit device includes a differential amplifier circuit that amplifies the read information produced on one of the first and second common data lines by a charge share with the read data line selected by the data line select circuit using the precharge voltage of the other of the first and second common data lines as the reference voltage.

6. A semiconductor integrated circuit device according to claim 1,

wherein the storage MOSFET is set to an OFF state regardless of the write information voltage in a write operation of the semiconductor integrated circuit,

wherein, in the read operation of the semiconductor integrated circuit device, the storage MOSFET is set to an ON or OFF state corresponding to the information held in the gate of the storage MOSFET by the transition of the word line from the first voltage to the second voltage.

7. A semiconductor integrated circuit according to claim I, wherein each of the plurality of word lines is coupled with the gate of the write transistor and the gate of the storage MOSFET.

8. A semiconductor integrated circuit device according to claim 1, wherein the write transistor is formed above the storage MOSFET.

9. A semiconductor integrated circuit device comprising:

a plurality of memory cells, each having a storage MOSFET holding an information in a gate of the storage MOSFET and a write transistor supplying a write information voltage corresponding to the information to the gate of the storage MOSFET; and

a plurality of word lines coupled with the plurality of memory cells,

wherein the write information voltage is selected from a first voltage and a second voltage greater than the first voltage corresponding to the information to be stored in the memory cell and is supplied to the gate of the storage MOSFET,

wherein, in a write operation of the semiconductor integrated circuit device, the storage MOSFET is set to an OFF state regardless of the write information voltage,

wherein, in a read operation of the semiconductor integrated device, the write information voltage is boosted by a transition of a voltage of the word lines,

wherein, when the write information voltage is the first. voltage, the storage MOSFET is set to the OFF state in the read operation, and

wherein, when the write information voltage is the second voltage, the storage MOSFET is set to an ON state in the read operation.

10. A semiconductor integrated circuit device according to claim 9, wherein each of the plurality of the memory cells further has a capacitor coupled between the gate of the storage MOSFET and a corresponding one of the plurality of word lines.

11. A semiconductor integrated circuit device according to claim 9, wherein the gate of the write transistor is coupled with a corresponding to one of the plurality of word lines.

12. A semiconductor integrated circuit device according to claim 9, further comprising:

a plurality of data lines coupled with corresponding ones of the plurality of the memory cells,

a data line select circuit selecting one of the plurality of the data lines; and

a first and a second data line being coupled with one of the plurality of the data lines selected by the data line select circuit,

wherein the first and second common data lines are precharged to a precharge voltage that is between a high level voltage and a low level voltage at a time of amplifying voltages on the first and the second common data lines, and

wherein the read information which appears on one of the first and second common data lines is amplified using the precharge voltage of the other of the first and second common data lines as a reference voltage.

13. A semiconductor integrated circuit device according to claim 12, wherein the plurality of data lines has a plurality of a write data lines and a plurality of a read data lines,

wherein each of the plurality of write data lines is coupled with the write transistor included in each of the plurality of memory cells, and

wherein each of the plurality of read data lines is coupled with the storage MOSFET in each of the plurality of memory cells.

14. A semiconductor integrated circuit device according to claim 13, further comprising:

a plurality of write control circuits connected between the plurality of read data lines and the plurality of write data lines, respectively,

wherein each of the plurality of write control circuits conveys a signal which appeared on a corresponding one of the plurality of read data lines to a corresponding one of the plurality of write data lines.

15. A semiconductor integrated circuit device according to claim 9, wherein the write transistor is formed above the storage MOSFET.

16. A semiconductor integrated circuit device comprising:

a memory array, wherein the memory array further includes; a plurality of memory cells, each having a storage MOSFET holding an information voltage in a gate of the storage MOSFET and set to an ON or OFF state according to the information voltage, and a write transistor supplying a write information voltage corresponding to the information voltage to the gate of the storage MOSFET;

a plurality of write data lines, each being applied with the write information voltages given as the information voltage of corresponding ones of the memory cells;

a plurality of read data lines, each being applied with a read information corresponding to the ON or OFF state of the storage MOSFET of the memory cells;

a word line structure connected to the plurality of memory cells;

a data line select circuit selecting one of the plurality of read data lines; and

first and second common data lines being connected to one of the read data lines selected by the data line select circuit,

wherein, during a non-select state, the write transistor is set to an OFF state and the storage MOSFET is set to on OFF state,

wherein, in a first select period, the write transistor is set to an OFF state, the read data line is discharged when the information voltage is high level or the read data line is not discharged when the information voltage is low level,

wherein, in a second select period, in which either the information voltage to be written into the write data lines or a read information voltage corresponding to the read information are applied, the write transistor is set to ON state,

wherein the first and second common data lines are precharged to a precharge voltage that is a voltage between a high level voltage and a low level voltage at a time of amplifying voltages on the first and the second common data lines in the non-select state, and

wherein the read information which appears on one of the first and second common data lines corresponding to a voltage which appeared on the read data line selected by the data line select circuit is amplified using the precharge voltage of the other of the first and second common data lines as a reference voltage.

17. A semiconductor integrated circuit device according to claim 16,

wherein the same number of data lines are respectively coupled with each of the first and second common data lines via the data line select circuit, and

wherein the semiconductor integrated circuit device includes a differential amplifier circuit that amplifies the read information produced on one of the first and second common data lines by a charge share with the read data line selected by the data line select circuit using the precharge voltage of the other of the first and second common data lines as the reference voltage.

18. A semiconductor integrated circuit device according to claim 17,

wherein the differential amplifier circuit includes a CMOS latch circuit having a pair of CMOS inverter circuits, the pair of CMOS inverter circuits having cross-coupled inputs and outputs, and an operating voltage of the CMOS latch circuit is supplied during amplification.

19. A semiconductor integrated circuit device according to claim 18, further comprising:

a write control circuit connected between the read data lines and the write data lines,

wherein the write control circuit applies the read information on the read data lines to the write data lines.

20. A semiconductor integrated circuit device according to claim 19, wherein the write control circuit is comprised of a transfer gate MOSFET connecting the read lines with the write data lines.